node between the first and second capacitors connected in series is set to a control voltage level that is sufficient to reduce the transient stress when the integrated circuit transitions to the low power state. When the circuit is in the high power state (e.g., active), the middle node is disconnected or isolated from the control voltage level. In one embodiment, as described above, a control device such as a switching transistor can be used to connect the middle node to or disconnect the middle node from the control voltage level, based upon the particular power state of the integrated circuit. The method **900** then proceeds to end at block **991**.

FIG. **10** shows a flow diagram of a method **1000** for balancing the system performance requirements (e.g., output voltage requirement) with the system constraints (e.g., die area, stress limitations of capacitors) in a charge pump circuit. The charge pump circuit in this embodiment includes a plurality of pump stages connected in series. Each pump stage includes an input node and an output node. The output node of each stage is coupled to the input node of a next stage. The input node of the first pump stage is coupled to a power supply to receive an input voltage. The output node of the last stage is coupled to a device that requires a higher voltage level than that provided by the power supply (e.g., a flash memory device). Again, it is assumed for the purposes of explanation and illustrations that there are two different types of capacitors (e.g., type one and type two) available for use as the storage and boot node capacitors in the charge pump circuit. It is assumed in this embodiment that type two capacitors can withstand more stress than type one capacitors but have larger die area than type one capacitors. In one embodiment, the type one capacitors are ONO capacitors and the type two capacitors are MOS capacitors. MOS capacitors can withstand more stress compared with ONO capacitors. However, MOS capacitors occupy more die area. The method **1000** starts at block **1001** and proceeds to block **1005**. At block **1005**, the voltage level at the output node of each pump stage in the charge pump circuit is determined. At decision block **1009**, the method **1000** proceeds to block **1013** if the output voltage level at the respective output node does not exceed the stress limitation or the breakdown voltage level of a single type one (e.g., ONO) capacitor. Otherwise the method **1000** proceeds to decision block **1017**. At block **1013**, a single type one (ONO) capacitor is used as the storage capacitor since it can withstand the stress. A single type one (ONO) capacitor is also used as the boot node capacitor. At decision block **1017**, the method **1000** proceeds to block **1021** if the output voltage at the respective output node does not exceed the stress limitation of a single type two capacitor (e.g., MOS capacitor). Otherwise the method **1000** proceeds to block **1023**. At block **1021**, a single type two capacitor (e.g., MOS capacitor) is used as the storage capacitor and a single type two capacitor is also used as the boot node capacitor in the respective pump stage. At block **1023**, since the output voltage at the respective output node exceeds the stress limitation of both a single type one and a single type two capacitor, a stacked capacitor configuration including two or more capacitors connected in series is needed to reduce the voltage across each individual capacitor. In this embodiment, a stacked capacitor configuration using type one capacitors is used since type one capacitors have smaller die area than type two capacitors. The number of type one capacitors to be connected in series in the stacked configuration depends upon the maximum voltage level at the respective output node. In this example it is assumed that two capacitors connected in series are sufficient. In one embodiment, the capacitors connected in series have the same capacitance to split the voltage equally across the individual capacitors. The method then proceeds from block **1023** to block **1025**. At block **1025**, to prevent the transient stress that can occur when the charge pump circuit transitions from one power state (e.g., full power, running, etc.) to another power state (e.g., shut down, powered off, standby, etc,) the middle node between the first and second capacitors connected in series is set to a control voltage level that is sufficient to reduce the transient stress when the integrated circuit transitions from a high power state to a low power state. In one embodiment, as explained above, the output node of at least the final stage in the charge pump circuit can go from a negative voltage level (e.g., −15 volts) when the charge pump circuit is running to a positive voltage level (e.g., +11 volts) when the charge pump circuit is shut down and then gets initialized to a proper voltage level, for example +5 volts. When this transition occurs, the total voltage sweep or the transient stress is 26 volts which exceeds the stress limitation of the capacitors even in the stacked configuration. To prevent this transient stress, the voltage level at the middle node between the two capacitors connected in series is dynamically controlled as described above. At decision block **1025**, the method **1000** proceeds to block **1029** if the charge pump circuit is in a low power state (e.g., shut down). Otherwise, the method **1000** proceeds to block **1033**. At block **1029**, the middle node is connected to a control voltage level that is sufficient to reduce the transient stress below the stress limitation of the capacitors. At block **1033**, the middle node is disconnected or isolated from the control voltage level. In one embodiment, as described above, a control device such as a switching transistor can be used to connect the middle node to or disconnect the middle node from the control voltage level, based upon the current state of the charge pump circuit (e.g., whether it is shut down or running). The method **1000** then proceeds to end at block **1091**.

The invention has been described in conjunction with the preferred embodiment. It is evident that numerous alternatives, modifications, variations and uses will be apparent to those skilled in the art in light of the foregoing description.

What is claimed is:

1. A method of controlling the voltage levels across capacitors coupled between a first node and a second node of an integrated circuit so that the voltage levels across these capacitors will not exceed the breakdown voltage limitation of these capacitors, the voltage level between the first and second nodes varying from a second voltage level to a first voltage level when the integrated circuit transitions from a second power state to a first power state, the first power state corresponds to a low power state and the second power state corresponds to a high power state, the method comprising:

connecting in series a first capacitor and second capacitor between the first and second nodes of the integrated circuit forming a middle node between the first and second capacitors; and

setting the voltage level of the middle node to a third voltage level when the integrated circuit is placed in the first power state such that the voltage level between the first and middle nodes does exceed the breakdown voltage of the first capacitor and the voltage level between the middle and second nodes does not exceed the breakdown voltage of the second capacitor.

2. The method of claim **1** wherein setting the voltage level of the middle node comprises:

connecting the middle node to a voltage source corresponding to the third voltage level in response to a

control signal indicating that the integrated circuit is placed in the first power state.

3. The method of claim 2 further comprising:

disconnecting the middle node from the voltage source in response to the control signal indicating that the integrated circuit is placed in the second power state.

4. The method of claim 3 wherein the control signal is set to a first value if the integrated circuit is in the first power state and set to a second value if the integrated circuit is in the second power state.

5. The method of claim 3 wherein connecting the middle node to the voltage source comprises:

turning on a switching device to connect the middle node to the voltage source.

6. The method of claim 5 wherein disconnecting the middle node from the voltage source comprises:

turning off the switching device to disconnect the middle node from the voltage source.

7. The method of claim 6 wherein the switching device comprises a transistor.

8. The method of claim 1 wherein the first and second capacitors are selected from the group consisting of oxide-nitride-oxide (ONO) capacitors and metal-oxide-semiconductor (MOS) capacitors.

9. The method of claim 1 wherein the capacitance of the first capacitor is approximately equal to the capacitance of the second capacitor.

10. A method of controlling the voltage levels across capacitors coupled between a first node and a second node of an integrated circuit so that the voltage levels across these capacitors will not exceed the breakdown voltage limitation of these capacitors, the voltage level between the first and second nodes varying from a second voltage level to a first voltage level when the integrated circuit transitions from a second power state to a first power state, the method comprising:

connecting in series a first capacitor and second capacitor between the first and second nodes of the integrated circuit forming a middle node between the first and second capacitors; and

setting the voltage level of the middle node to a third voltage level when the integrated circuit is placed in the first power state such that the voltage level between the first and middle nodes does exceed the breakdown voltage of the first capacitor and the voltage level between the middle and second nodes does not exceed the breakdown voltage of the second capacitor, the third voltage level at the middle node corresponds to the voltage level at the first node when the integrated circuit is placed in the first power state.

11. The method of claim 10 wherein the middle node is connected to the first node via a switching device when the integrated circuit is placed in the first power state.

12. The method of claim 11 wherein the middle node is disconnected from the first node via the switching device when the integrated circuit is placed in the second power state.

13. The method of claim 12 wherein the switching device is turned on in response to a control signal indicating that the integrated circuit is in the first power state and turned off in response to the control signal indicating that the integrated circuit is in the second power state.

14. The method of claim 13 wherein the switching device comprises a transistor.

15. In a charge pump having a plurality of pump stages connected in series, at least one of the pump stages including at least one node to be coupled to a corresponding clock signal via a capacitive device, the at least one node having a first voltage when the charge pump is in a first power state and a second voltage when the charge pump is in a second power state, a method of balancing the voltage requirement at the at least one node with the stress limitation and die area of the capacitive device, the method comprising:

using a single capacitor of a first type as the capacitive device between the at least one node and the corresponding clock signal if the first voltage and second voltage do not exceed the stress limitation of the single capacitor of the first type;

if the second voltage exceeds the stress limitation of the single capacitor of the first type, using a single capacitor of a second type as the capacitive device between the at least one node and the corresponding clock signal if the first voltage and second voltage do not exceed the stress limitation of the single capacitor of the second type, the single capacitor of the second type having greater stress limitation and greater die area than the single capacitor of the first type; and

if the second voltage exceeds the stress limitation of the single capacitor of the second type, using two capacitors of the first type connected in series as the capacitive device between the at least one node and the corresponding clock signal if the first voltage and second voltage do not exceed the combined stress limitation of the two capacitors of the first type; and

if the first voltage exceeds the combined stress limitation of the two capacitors of the first type, setting the middle node between the two capacitors of the first type to a third voltage level when the charge pump is in the first power state such that the voltage across each of the two capacitors does not exceed the stress limitation of the respective capacitor, the third voltage level at the middle node corresponds to the voltage level at the first node when the charge pump is placed in the first power state.

16. The method of claim 15 wherein setting the middle node between the two capacitors to the third voltage level comprises:

connecting the middle node to a voltage source corresponding to the third voltage level via a switching device in response to a control signal indicating that the charge pump is placed in the first power state.

17. The method of claim 15 further comprising:

disconnecting the middle node from the voltage source corresponding to the third voltage level via the switching device in response to the control signal indicating that the charge pump is placed in the second power state.

18. A charge pump circuit including a plurality of pump stages being connected in series each having an input node and an output node, at least one of the pump stages comprising:

a switching transistor having a gate, a first terminal, and a second terminal, the first terminal being coupled to the input node of the respective pump stage and the second terminal being coupled to the output node of the respective pump stage;

a first capacitor having a first end and a second end, the first end of the first capacitor being coupled to the gate of the switching transistor;

a second capacitor having a first end and a second end, the first end of the second capacitor being coupled to the second end of the first capacitor forming a first inter-

mediate node, the second end of the second capacitor being coupled to a first clock signal;

a third capacitor having a first end and a second end, the first end of the third capacitor being coupled to the output node of the respective pump stage; and

a fourth capacitor having a first end and a second end, the first end of the fourth capacitor being coupled to the first end of the third capacitor forming a second intermediate node, the second end of the fourth capacitor being coupled to a second clock signal

wherein the first and second intermediate nodes are set to a predetermined voltage level when the charge pump circuit is placed in a low power state.

19. The charge pump circuit of claim **18** wherein the first and second intermediate nodes are set to the predetermined voltage level via a switching device in response to a control signal indicating that the charge pump circuit is placed in the low power state.

20. The charge pump circuit of claim **19** wherein the switching device comprises a first control transistor and a second control transistor, the first and second control transistors being turned on in response to the control signal indicating that the charge pump circuit is placed in the low power state to connect the first intermediate and second intermediate nodes, respectively, to a voltage source corresponding to the predetermined voltage level.

21. The charge pump circuit of claim **20** wherein the voltage source is set to a first voltage level to turn on the first and second control transistors when the charge pump circuit is placed in the low power state and to a second voltage level to turn off the first and second control transistors when the charge pump circuit is placed in a high power state.

22. A charge pump stage in a charge pump circuit, the charge pump stage comprising:

a first switching transistor having a gate, a first terminal and a second terminal, the first terminal being coupled to an input node of the charge pump stage, the second terminal being coupled to an output node of the charge pump stage;

at least two capacitors connected in series between the gate of the first switching transistor and a first clock signal forming a first intermediate node between the two capacitors;

at least two capacitors connected in series between the output node and a second clock signal forming a second intermediate node between the two capacitors;

a control device to connect the first and second intermediate nodes to a first voltage source when the charge pump circuit is in a first power state and to disconnect the first and second intermediate nodes from the first voltage source when the charge pump circuit is in a second power state;

a first diode having an input terminal and an output terminal, the input terminal being coupled to the first terminal of the first switching transistor and the output terminal being coupled to the gate of the first switching transistor; and

a second diode having an input terminal and an output terminal, the input terminal being coupled to the gate of the first transistor, the output terminal being coupled to the first terminal of the first switching transistor.

23. The charge pump stage of claim **22** wherein the control device comprises a first control transistor and a second control transistor, the first and second control transistors being turned on in response to a control signal indicating that the charge pump circuit is in the first power state, the first and second control transistors being turned off in response to the control signal indicating that the charge pump circuit is in the second power state.

24. The charge pump stage of claim **23** wherein the first voltage source is used as the control signal, the first voltage source being set to a first value when the charge pump circuit is in the first power state and being set to a second value when the charge pump circuit is in the second power state.

* * * * *